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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/940,709	GSCHWIND ET AL.	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *10 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 8, 15 – 20, 22, 23, 25 – 34, and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Kumar (US Patent No. 6,678,790).

3. With respect to claims 1, 2, 22, 26, 29, 30 and 33, Kumar discloses a data storage system (figure 1), comprising:

at least one microprocessor (figure 1a, 26); and

a configurable memory (12), integrated with the at least one processor, for servicing the at least one microprocessor in a first mode of operation that emulates a local, non-cache memory and a second mode of operation that emulates a cache (abstract), wherein the configurable memory comprises a memory portion for storing tag bits (figure 2, 50) and data bits in a single logical line (col. 3, lines 32 – 33), in the second mode of operation, and

wherein a selection of any of the first mode of operation and the second mode of operation is capable of being overridden by another selection of an other of the first mode of operation and the second mode of operation (col. 2, lines 47 – 51).

4. With respect to claim 3, wherein the configurable memory is capable of having either the first mode of operation or the second mode of operation selected at a burn-in time (mode selection is under software control, making the mode selection possible anytime while the system is up and running, including "a burn-in time", i.e. a period of initial operation of a new device).

5. With respect to claim 4, the configurable memory is capable of having either the first mode of operation or the second mode of operation selected at a power-up time (col. 2, lines 51 – 55).

6. With respect to claim 5, the first mode of operation or the second mode of operation is selected at the power-up time using an external signal (col. 2, lines 51 – 55).

7. With respect to claim 6, the configurable memory is capable of having either the first mode of operation or the second mode of operation selected during a program execution (col. 2, lines 47 – 48).

8. With respect to claim 7, the first mode of operation or the second mode of operation is selected during the program execution based upon a value of a special configuration register (col. 2, lines 47 – 48).

9. With respect to claim 8, the first mode of operation or the second mode of operation is selected during the program execution based upon a value of an external signal (col. 2, lines 48 – 51, control register is loaded by the CPU which is external to the memory).

10. With respect to claims 15 and 23, the configurable memory comprises:

a memory array (figure 2, 52); and

memory configuration logic for selecting the first mode of operation or the second mode of operation (figure 1, 16, figure 2, 58).

11. With respect to claim 16, the configurable memory is capable of selecting one of a local memory read mode and a local memory write mode in the first mode of operation and is further capable of selecting one of a cache read mode and a cache write mode in the second mode of operation (read mode, i.e. mode of operation while reading, and write mode, i.e. mode of operation while writing, are inherent in this type of memory, either in cache mode or local memory mode).

12. With respect to claim 17, the selection may be overridden by the other selection dynamically (col. 2, lines 47 – 51).

13. With respect to claim 18, the configurable memory comprises a plurality of static random access memory cells (col. 3, lines 34 – 35).

14. With respect to claim 19, the configurable memory comprises a plurality of dynamic random access memory cells (col. 3, lines 34 – 35).

15. With respect to claim 20, the configurable memory is capable of being dynamically employed as a sole memory (abstract, main memory) serving the processor and as a portion of a larger, memory hierarchy (abstract, cache, see also col. 1, lines 18 – 24, cache is a portion of a larger memory hierarchy that includes a cache memory and a main memory).

16. With respect to claim 25, the memory system further comprises:

tag match logic for determining a match between the stored tag bits and bits corresponding to a memory access (figure 12, 80, 82); and

at least one multiplexer (44) for selecting and outputting data corresponding to the memory access, when the match is determined.

17. With respect to claims 27, 28, 31, 32, and 34, the at least one microprocessor and the configurable memory array are integrated on a single chip/package (figure 1a, see also col. 2, lines 33 – 35).

18. With respect to claim 37, said integrating step integrates the at least one microprocessor (figure 1b, 26) with the configurable memory based upon a multi-chip (11 and 13) module.

19. Claims 1, 6, 9 – 14, 21, and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Ramagopal *et al.* (US Patent No. 6,606,684, hereinafter "Ramagopal").

20. With respect to claim 1, Ramagopal discloses a memory system on a chip (figure 1, 100, col. 2, lines 38 – 39), comprising:

a configurable memory (106) having a first mode of operation wherein the configurable memory is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory (col. 3, lines 28 – 29), and

wherein a selection of any of the first mode of operation and the second mode of operation is capable of being overridden by an other selection of an other of the first mode of operation and the second mode of operation (col. 4, lines 51 – 52, selection is programmable).

21. With respect to claim 6, the configurable memory is capable of having either the first mode of operation or the second mode of operation selected during a program execution (see rejection of claim 1 above, the selection is programmable).

22. With respect to claim 9, the first mode of operation or the second mode of operation is selected during the program execution based upon a supplied address (col. 4, lines 60 – 62).

23. With respect to claim 10, the configurable memory is capable of having either the first mode of operation or the second mode of operation selected based upon a result of comparing a supplied address to a range of addresses (col. 4, lines 51 – 65).

24. With respect to claim 11, the range of addresses are determined at a burn-in time (mode selection, i.e. bank selection, is programmable, making the selection possible anytime while the system is up and running, including "a burn-in time", i.e. a period of initial operation of a new device).

25. With respect to claim 13, the range of addresses are determined dynamically (the bank selection is programmable).

26. With respect to claim 14, the system further comprises:

a configuration register for storing the range of addresses (figure 6, 602, 604).

27. With respect to claim 21, the first mode of operation and the second mode of operation are employed concurrently (col. 4, table 1, memory configuration 2).

28. With respect to claim 29, Ramagopal discloses a memory system on a chip (figure 1, 100), comprising:

a processor (102); and

a configurable memory (106) having three modes of operation, a first mode of operation for emulating a local, non-cache memory (col. 4, table 1, memory configuration 0), a second mode of operation for emulating a cache memory (table 1, memory configuration 3), and a third mode of operation for emulating both the local memory and the cache (table 1, memory

configuration 2), wherein any of the three modes of operation may be selected at any given time (col. 4, lines 51 – 52).

29. Claims 12 is rejected under 35 U.S.C. 102(e) as being anticipated by Baltz (US Patent No. 6,321,318).

Baltz discloses a memory system on a chip (abstract), comprising:

a configurable memory having a first mode of operation wherein the configurable memory is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory, and

wherein a selection of any of the first mode of operation and the second mode of operation is capable of being overridden by an other selection of an other of the first mode of operation and the second mode of operation (col. 2, lines 18 – 28, see also claim 1),

wherein the configurable memory is capable of having either the first mode of operation or the second mode of operation selected based upon a result of comparing a supplied address to a range of addresses (col. 2, lines 38 – 41),

wherein the range of addresses are determined at a boot-up time (col. 2, lines 31 – 32).

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar in view of Lehmann (US Patent No. 6,355,968).

Kumar discloses all of the limitations of the parent claim as discussed above. However, Kumar does not specifically disclose the use of a fuse to configure the system. On the other hand, Lehmann discloses the use of fuses to configure semiconductor circuits (col. 1, lines 10 – 15).

It would have been obvious to one of ordinary skill in the art, having the teachings of Kumar and Lehmann before him at the time the invention was made, to use the semiconductor circuit configuration using fuses teachings of Lehmann in the configurable semiconductor memory circuit of Kumar, in order to fabricate the chip using an area efficient wiring scheme (Lehmann, col. 1, lines 5 – 7).

32. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar in view of Sample *et al.* (US Patent No. 6,377,912, hereinafter "Sample"), or in the alternative, in view of Natarajan (US Patent No. 6,611,796).

Kumar discloses all of the limitations of the parent claim as discussed above. However, Kumar does not specifically disclose macro cells to implement memory system. On the other hand, Sample (col. 29, lines 11 – 17, col. 31, lines 27 – 33) and Natarajan (col. 4, lines 16 – 23) disclose the use of macro cells in IC memory chip designs.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kumar and Sample or Natarajan before him at the time the invention was made, to use the design techniques using macros teachings of Sample or Natarajan in the design of Kumar's system, in order to be able to verify electronic circuit designs before fabrication (Sample 16 – 18, Natarajan 23 – 26).

33. Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar in view of Isaak (US Patent No. 6,426,549).

Kumar discloses all of the limitation of the parent claim as discussed above. However, Kumar does not specifically disclose methods of integrating the claimed memory package using a chip stack and a flip chip techniques. On the other hand, Issak discloses both of these techniques (abstract).

It would have been obvious to one of ordinary skill in the art, having the teachings of Kumar and Isaak before him at the time the invention was made, to use the IC packaging teachings of Isaak to make the configurable memory IC of Kumar, in order to be able to actually produce the memory devices. Isaak's method uses available materials and known process techniques and is suitable for automated production methods (col. 3, lines 49 – 53).

Response to Amendment

34. Claim 3 has been amended to overcome rejections under U.S.C. 112, first and second paragraphs. Corresponding rejections are withdrawn.

Response to Arguments

35. Applicant's arguments filed September 10, 2004, have been fully considered but they are not persuasive. Applicant's argument regarding "tag bits and data bits in a single logical line" in a cache mode is ineffective since Kumar discloses such a feature as shown above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

whc
October 28, 2004

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